CLAIMS

Having thus described our invention, what we claim as new, and desire to secure by Letters Patent is:

1. A dual port SRAM cell comprising six nMOS devices,
two nMOS pull-down devices,
two nMOS first pair of transfer devices,
two nMOS second pair of transfer devices,
a first pair of bitlines coupled to the drains of the first pair of transfer devices,
a second pair of bitlines coupled to the drains of the second pair of transfer devices,
a first wordline coupled to the gates of the first pair of transfer devices, and
a second wordline coupled to the gates of the second pair of transfer devices.

2. The dual port SRAM cell of claim 1, wherein said first pair of transfer gates also serve as the load devices for the SRAM cell.

3. The dual port SRAM cell of claim 1, wherein said second pair of transfer gates also serve as the load devices for the SRAM cell.

4. The dual port SRAM cell of claim 1, wherein said first wordline is the first port for read and write operations.

5. The dual port SRAM cell of claim 1, wherein said second wordline is the second port for read and write operations.

6. A dual port SRAM cell comprising four nMOS and three pMOS devices,

two nMOS pull-down devices,

two pMOS pull-down devices,

two nMOS first pair of transfer devices,

one pMOS second transfer device,

a first pair of bitlines coupled to the drains of the first pair of transfer devices,

a second bitline coupled to the drain of the second transfer device,

a first wordline coupled to the gates of the first pair of transfer devices, and

a second wordline coupled to the gate of the pMOS second transfer device.

7. The dual port SRAM cell of claim 6, wherein said first wordline is the first port for read and write operations.

8. The dual port SRAM cell of claim 6, wherein said second wordline is the second port for read-only operations.

9. A high-speed SRAM architecture comprising:

two dual port SRAM blocks,

a TAG cache, and

an interface circuit.

10. The high-speed SRAM architecture of claim 9, wherein a write operation is performed with a first ½ cycle writing data to the first dual port cache, and a second ½ cycle writing data to the second dual port cache via the read-write port.

11. The high-speed SRAM architecture of claim 9, wherein a read operation is performed with a first ½ cycle reading data from the first dual port cache, and a second ½ cycle reading data from the second dual port cache via either of the dual ports.

12. The high-speed SRAM architecture of claim 9, wherein the addresses of valid data stored in the dual dual-port SRAM cache are stored in the TAG cache, incoming addresses are compared to addresses stored in the TAG and to schedule read and write operations, and when new data is stored in the dual dual-port cache, the status in the TAG cache is updated.